OPTIMIZATION OF CMOS DEVICES IN MULTI VALUED LOGIC DECODER

Vinay U. Kale Dr. Vijay T. Ingole Vikram S. Ingole

Abstract - The design of multi valued logic decoder is constructed using different building blocks of ternary switches. The building blocks of ternary switches are implemented by padding a CMOS device. The main objective is to optimize the CMOS devices in the design of multi valued logic decoder. This multi valued logic decoder is provided with three different logic levels. The design is based on familiar binary switching circuit elements and optimization techniques. The design leads to a simple circuit's realization. The multi valued logic decoder is the basic building block of binary to ternary converter and vice – versa. The design is implemented using cadence schematic editor and simulated using cadence virtuoso analog design environment at 180nm CMOS process technology.

Index Terms— CMOS, Decoder, Multi valued LOGIC, MVL, NMOS, PMOS, Threshold voltage, Ternary.

1 INTRODUCTION

The 3 switching levels (3 Valued) are named with ternary as a part of Multi Valued Logic (MVL). The three switching levels are referred as "0", "1" and "2", signifies the low, intermediate and high voltage levels [11].

It can be summarized as reductions in the interconnections require to implement logic functions, thereby reducing chip area, more information can be transmitted over a given set of lines, lesser memory requirement for a given data length[13].

The binary logic is having certain disadvantages that correspond to interconnection. Therefore Multi Valued Logic mainly known as the higher radix logic has been implemented. The approach of Multi Valued Logic is more advantageous over binary counterparts. Due to this Multi Valued Logic is preferred in the designing of digital systems [1].

To emulate the multi valued function MVL decoder has been designed. For the efficient implementation of multi valued logic the devices should be in multi valued in nature.

The multi valued logic provides motivation in designing of various ternary logic gates like ternary NAND, ternary AND, ternary XOR and ternary OR also binary to ternary and ternary to binary converter as well [4].In this paper we have shown transient analysis of proposed ternary decoder with different building blocks of ternary switches.

2 TERNARY SWITCHING ALGEBRA

Unsymmetrical Ternary Logic levels i.e. 0, 1 and 2 are used to establish the characteristics of the CMOS transistors. The ternary logic levels 0, 1 and 2 are referred as a 0V, 1V, and 2V [8]. The basic building block of different Ternary-Switches model is design to characterize switching properties of the CMOS transistors [2].

The switching properties of the CMOS transistors is realized with NMOS and PMOS where it is assumed that the threshold voltage should be minimum than 1 V [7].

For the NMOS the gate terminal (X) is used as controlling independent input terminal. The second terminal of NMOS named as source (Y) connected independent inputs whereas the output is taken from drain terminal (Z). The substrate of NMOS is to be connected always to low voltage level. The terminal gate and source belongs to ternary logic (0, 1, and 2). The behavior of NMOS for the above configuration is simulated which are as follows. The symbol of NMOS and PMOS is shown in figure 1 &2.

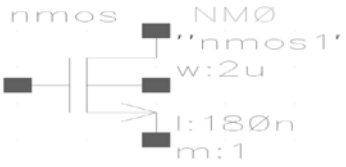

FIG.1. SYMBOL OF NMOS

i) If X=0 then=>n1

Z= floating (Y=0);

ii) If X=1 then=>n2

Z= 0 (Y=0);

iii) If X=2 then=>n3

Z= 0 (Y=0);

iv) If X=0 then=>n4

Z= floating (Y=2);

v) If X=1 then=>n5

Z= floating (Y=2);

vi) If X=2 then=>n6

Z= 2(U) (Y=2)

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The same argument mentioned in the NMOS case is applicable except for the threshold voltage less than negative 1 V and the substrate has to be connected to the highest voltage level i.e. 2V [5].

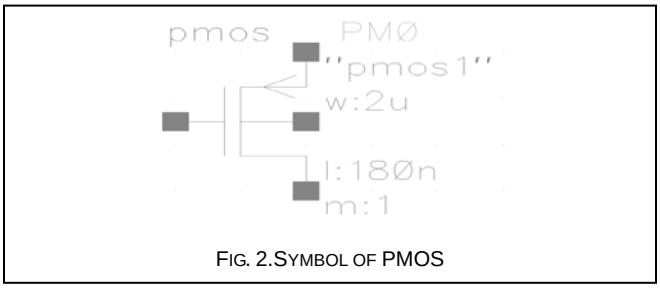

FIG. 2.SYMBOL OF PMOS

i) If X=0 then=>p1

Z= 2 (Y=2);

ii) If X=1 then=>p2

Z= 2 (Y=2);

ii) If X=2 then=>p3

Z=floating (Y=2);

2.1BUILDING BLOCK OF TERNARY SWITCHES

The design of switch1 is shown in fig.3 (a). In this design PMOS is padded to get high logic level for intermediate level

TABLE 1: Truth table of switch1

INPUT	OUTPUT
0	2
1	0
2	0

otherwise complement output. Table 1 may be expressed as follows, by making use of padding of CMOS devices in the complementary CMOS inverter [2].

The equation 1, 2 & 3 defined switch1 as follows.

$$X^0(2) = p1 + n1 \quad (1)$$

$$X^1(0) = p2 + n2 \quad (2)$$

$$X^2(0) = p3 + n3 \quad (3)$$

The design of switch2 is shown in fig.3 (b). The circuit design is same as switch1 only padding of NMOS is take place in switch2. The truth table of Switch2 is shown in Table 2.

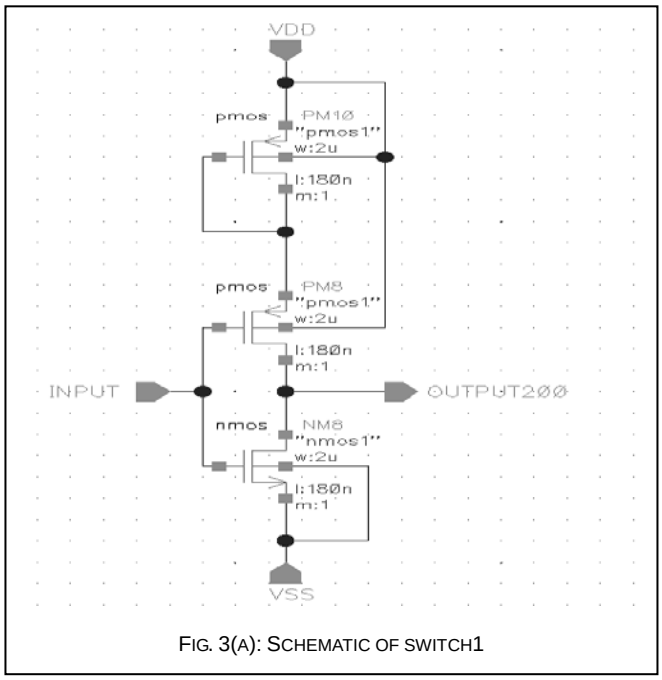

FIG. 3(A): SCHEMATIC OF SWITCH1

TABLE 2: Truth table of switch2

INPUT	OUTPUT
0	2
1	2
2	0

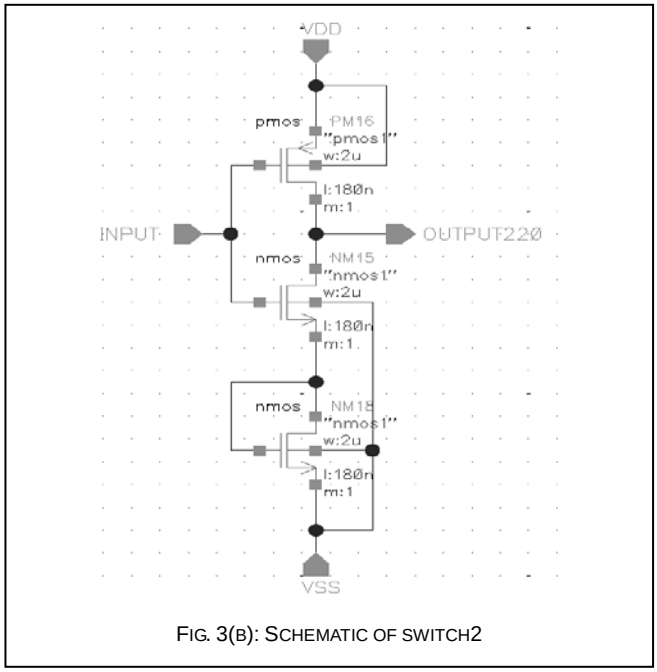

FIG. 3(B): SCHEMATIC OF SWITCH2

Similarly the switch2 is described by equation 4, 5 and 6.

$$X^0(2) = p3 + n4 \quad (4)$$

$$X^1(2) = p2 + n5 \quad (5)$$

$$X^2(0) = p3 + n6 \quad (6)$$

Switch3 circuit is nothing but a complementary CMOS inverter with source of NMOS is connected to output of switch1 for the input (2, 2, 0). The schematic of switch3 is shown in fig.3(c) equation 7, 8 and 9 defines the switch3 for the desired outputs. The truth table of Switch3 is shown in Table 3.

TABLE 3: Truth table of switch3

INPUT	OUTPUT
0	2
1	0
2	2

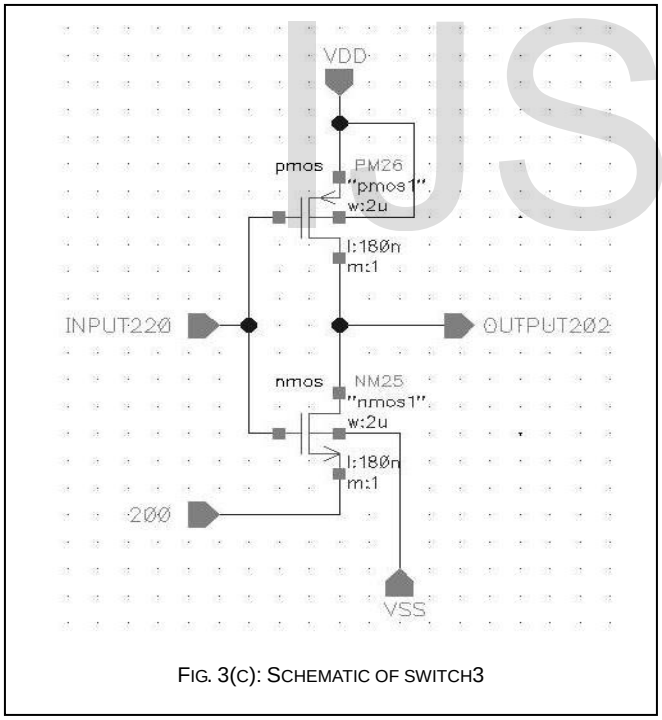

FIG. 3(C): SCHEMATIC OF SWITCH3

$$X^2(2) = p3 + n6 \quad (7)$$

$$X^2(0) = p3 + n3 \quad (8)$$

$$X^0(2) = p1 + n3 \quad (9)$$

3. PROPOSED DECODER

The proposed multi valued decoder is composed of three different ternary switches. Here padding of two MOS transistor is used.

This decoder is composed of total 10 transistors. Threshold voltage of switches is adjusted by padding of MOS transistors. By padding of PMOS in switch1, the input falls to low level. On the other hand if NMOS is considered the input is raised to high level. The desired ternary logic level is obtained by changing the threshold of a transistor.

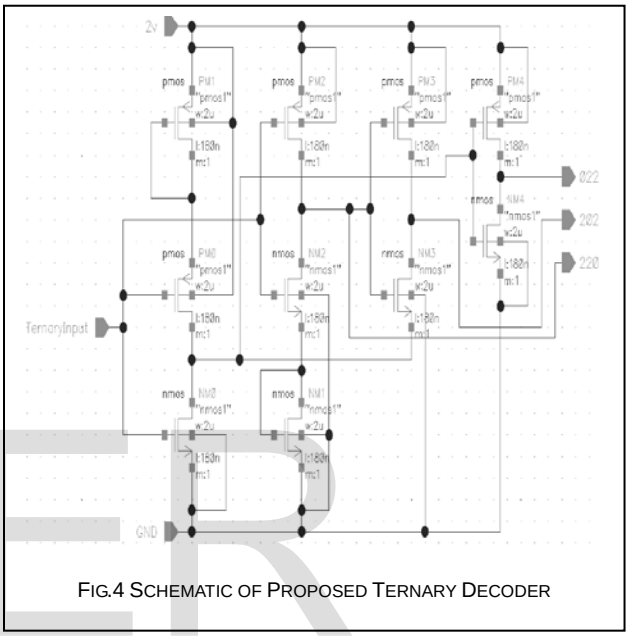

FIG.4 SCHEMATIC OF PROPOSED TERNARY DECODER

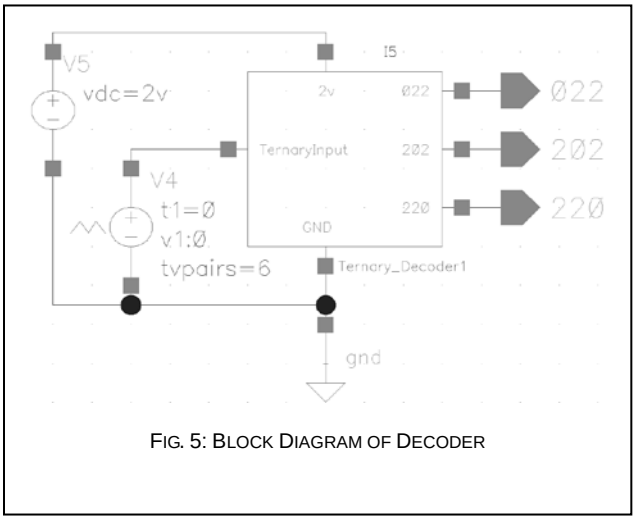

FIG. 5: BLOCK DIAGRAM OF DECODER

4. SIMULATION RESULT

In this paper for the implementation of proposed multi valued logic decoder and building blocks ternary switches, the Cadence schematic editor and cadence virtuosos analog design environment are used. The transient responses of above

designs are shown in figure 6, 7, 8 & 9.

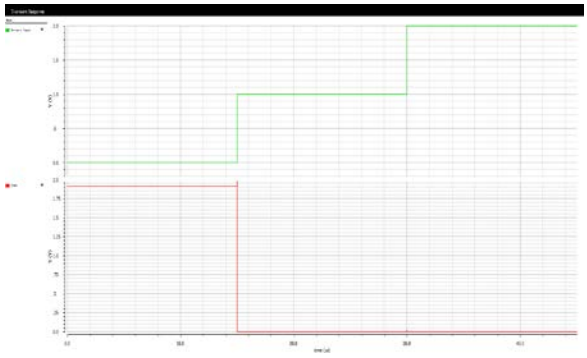

FIG. 6: TRANSIENT RESPONSE OF SWITCH1

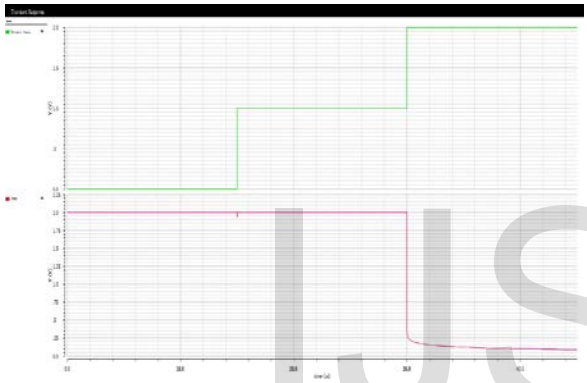

FIG. 7: TRANSIENT RESPONSE OF SWITCH2

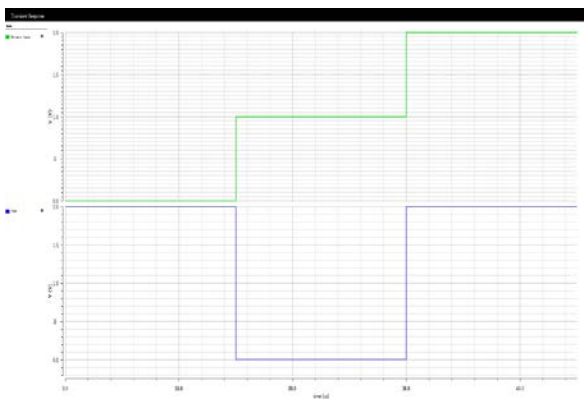

FIG. 8: TRANSIENT RESPONSE OF SWITCH3

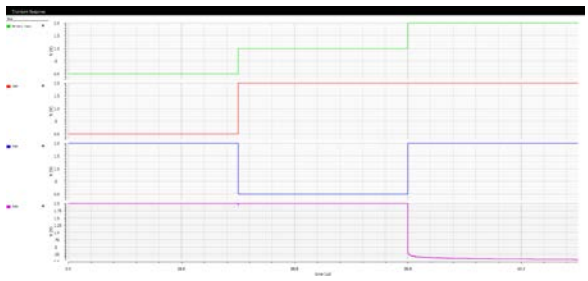

FIG. 9: TRANSIENT RESPONSE OF DECODER

5. CONCLUSION

The design of optimization of multi valued decoder is described. The proposed decoder is successfully implemented and simulated. It was seen that the number of gates required are less hence increases the speed of operation. In the verification through simulation, proposed multi valued decoders have fair result like speed of operation. This decoder is designed with 10 MOS transistor which reduces the chip area of device.

REFERENCES

[1] Mrs. Rawnaq A. Habeeb "Coding-Decoding Ternary Logic" Electrical Engineering Department/College of Engineering/ Basrah University/Iraq Iraq J. Electrical and Electronic Engineering Vol.10 No.1, 2014.

[2] Mudhafar A. Hassan Ali, Student Member, Zeee, Falah J. Hassan-Alshiroofi and Hemant G. Rotithor, senior member, "A Framework for Design of Multivalued Logic Functions and Its Application using CMOS Ternary Switches" IEEE transactions on circuits and systems-i: fundamental theory and applications, vol. 43, no. 4, April 1996.

[3] Meruva Kumar Raja*, Neelima Koppala** Meruva Kumar Raja et al "Modeling and Implementation of Reliable Ternary Arithmetic and Logic Unit Design using Vhdl" int. Journal of engineering research and applications ISSN: 2248-9622, vol. 4, issue 6(version 5), June 2014, pp.259-264.

[4] X.w. Wu Prof. F.p. Prosser "CMOS Ternary Logic Circuits". PhD IEE proceedings, vol. 137, pt. G, no. I, February 1990.

[5] Alex Heung and H. T. Mouftah "Depletion/Enhancement CMOS for A Low Power Family of Three-Valued Logic Circuits", senior member, IEEE journal of solid-state circuits, vol sc-20, no 2, April 1985.

[6] M. Yoeli and G. Rosenfeld, "Logical Design of Ternary Switching Circuits" Member, IEEE transactions on electronic computers February 1965.

[7] H. T. Mouftah and I. B. Jordan "Design of Ternary COS/MOS Memory and Sequential Circuits" IEEE transactions on computers, March 1977.

[8] Vani H Assistant Professor Dept of ECE ,Rymec Ballari Renuka Sagar Assistant Professor Dept of ECE Bitm Ballari Rohini H M Assistant Professor Dept of ECE Rymec Ballari " Multiplexer Based Design for Ternary Logic Circuits, international jour-

nal of computer applications (0975 – 8887) national conference on electronics and communication (NCEC 2015).

[9] Monika Nagaria1, Priyanka Goyal 2 “A Low Power Design Approach for the Implementation of Ternary Logic” HCTL open international journal of technology innovations and research (IJTIR) volume 14, April 2015 E-ISSN: 2321-1814, ISBN (print): 978-1-62951-946-3.

[10] Prashant S Wankhade, Dr Gajanan Sarate “Optimization of Ternary Combinational System” International Journal of Scientific & Engineering Research, Volume 6, Issue 5, May-2015 Issn 2229-5518 IJSER © 2015.

[11] Moiez a. Tapia “Solution of multivalued logic algebra equations” Electrical & Computer Engineering University O F M I A M I Coral Gables, Florida Proceedings - 1989 Southeastcon Ch2674-5/89/0000-0245$01.0001989 IEEE.

[12] K. C. Smith “The Prospects for Multivalued Logic: A Technology and Applications View”, fellow, IEEE, IEEE transactions on computers, vol. C-30, no. 9, September 1981.

[13] A.P.Dhande and V.T.Ingole “Design of 3-Valued R-S & D Flip – Flops Based on Simple Ternary Gates” World Academy of Science, Engineering and Technology 4 2005.